IN THE CLAIMS

Please amend the claims as follows.

1. (Original) A method for fabricating a raised source/drain of a semiconductor device, comprising:

forming a gate structure on a substrate;

forming a source/drain with a shallow-junction in the substrate beside the gate structure;

forming a spacer on sidewalls of the gate structure; and

forming an elevated SiGe layer on the gate structure and the source/drain with a shallow junction, wherein the elevated layer formed on the source/drain serves as an elevated source/drain layer.

2. (Original) The method of claim 1, wherein forming the elevated SiGe layer comprises performing rapid thermal chemical vapor deposition (RTCVD) to form the elevated SiGe layer.

3. (Original) The method of claim 2, wherein the RTCVD uses a reaction gas comprising Si_2H_6/GeH_4 mixture gas or SiH_2Cl_2/GeH_4 mixture gas.

4. (Original) The method of claim 2, wherein the RTCVD is conducted under 1~20 Torr and 500°C.

5. (Original) The method of claim 1, wherein a thickness of the elevated SiGe layer is 200~500Å.

6. (Original) The method of claim 1, further comprising performing an implantation to dope the elevated SiGe layer.

7. (Original) The method of claim 1, further comprising forming a metal silicide layer on the elevated SiGe layer.

8. (Original) The method of claim 7, wherein the metal silicide layer comprises cobalt silicide ($CoSi_x$) or nickel silicide ($NiSi_x$).

Claim 9 is (canceled).

10. (Currently Amended) A method for fabricating a raised source/drain of a semiconductor device, comprising:

forming a gate structure on a substrate, the gate structure having a capping layer thereon;

forming a source/drain with a shallow-junction in the substrate beside the gate structure, wherein an implanting energy for forming the source/drain with a shallow junction is 2~3 KeV;

forming a spacer on sidewalls of the gate structure; and

forming an elevated SiGe source/drain layer on the source/drain with a shallow junction.

11. (Original) The method of claim 10, wherein forming the elevated SiGe source/drain layer comprises performing rapid thermal chemical vapor deposition (RTCVD) to form the elevated source/drain layer.

12. (Original) The method of claim 11, wherein the RTCVD uses a reaction gas comprising Si_2H_6/GeH_4 mixture gas or SiH_2Cl_2/GeH_4 mixture gas.

13. (Original) The method of claim 11, wherein the RTCVD is conducted under 1~20 Torr and 500°C.

14. (Original) The method of claim 10, wherein a thickness of the elevated SiGe source/drain layer is 200~500Å.

15. (Original) The method of claim 10, further comprising performing an implantation to dope the elevated SiGe source/drain layer.

16. (Original) The method of claim 10, further comprising forming a metal silicide layer on the elevated SiGe source/drain layer.

17. (Original) The method of claim 16, wherein the metal silicide layer comprises cobalt silicide ($CoSi_x$) or nickel silicide ($NiSi_x$).

Claim18 is (canceled).

19. (Original) The method of claim 10, wherein the capping layer and the spacer comprise the same material.

20. (Original) The method of claim 19, wherein the capping layer and the spacer both comprise silicon nitride.

21. (Original) A method for fabricating a raised source/drain of a semiconductor device, comprising:

forming a gate structure on a substrate, the gate structure having a capping layer thereon;

forming a source/drain with a shallow-junction in the substrate beside the gate structure;

forming a spacer on sidewalls of the gate structure;

forming an elevated SiGe source/drain layer on the source/drain with a shallow junction;

removing the capping layer; and

forming a metal silicide layer on the gate structure and the elevated SiGe source/drain layer.

22. (Original) The method of claim 21, wherein forming the elevated SiGe source/drain layer comprises performing rapid thermal chemical vapor deposition (RTCVD) to form the elevated source/drain layer.

23. (Original) The method of claim 22, wherein the RTCVD uses a reaction gas comprising Si_2H_6/GeH_4 mixture gas or SiH_2Cl_2/GeH_4 mixture gas.

24. (Original) The method of claim 22, wherein the RTCVD is conducted under 1~20 Torr and 500°C.

25. (Original) The method of claim 21, wherein a thickness of the elevated SiGe source/drain layer is 200~500Å.

26. (Original) The method of claim 21, further comprising performing an implantation to dope the elevated SiGe source/drain layer.

27. (Original) The method of claim 21, wherein the metal silicide layer comprises cobalt silicide ($CoSi_x$) or nickel silicide ($NiSi_x$).

28. (Original) The method of claim 21, wherein an implanting energy for forming the source/drain with a shallow junction is 2~3 KeV.

29. (Original) The method of claim 21, wherein the capping layer and the spacer comprise different materials.

30. (Original) The method of claim 29, wherein the capping layer comprises silicon oxide and the spacer comprise silicon nitride.